SoundPort Controller

AD1812

FEATURES

Compatibility with:
- **Sound Blaster Pro***
- **AdLib***
- **Windows* Sound System**

16-Bit ΣΔ Stereo Codec
MPC Level-2+ Mixer
Dual DMA/Full Duplex Operation
On-Chip FIFO Buffers
Sample Rates from 5.5 kHz to 50 kHz
ADPCM Compression/Decompression
Plug and Play Compliant
Compatible MIDI MPU-401 Port
Integrated Game Port
Free Supporting Software:
- **Windows 3.1 Driver**
- **Windows 95 Driver**
- **Control Applets**
- **Diagnostics**

Power Management Modes
Operation from +5 V Supply
16-Bit Parallel Interface to ISA Bus
24 mA Bus Drive Capability

*Sound Blaster Pro is a trademark of Creative Labs, Ltd.
AdLib is a trademark of AdLib Multimedia.
Windows is a trademark and Microsoft is a registered trademark of Microsoft Corp.
SoundPort is a registered trademark of Analog Devices, Inc.

PRODUCT OVERVIEW

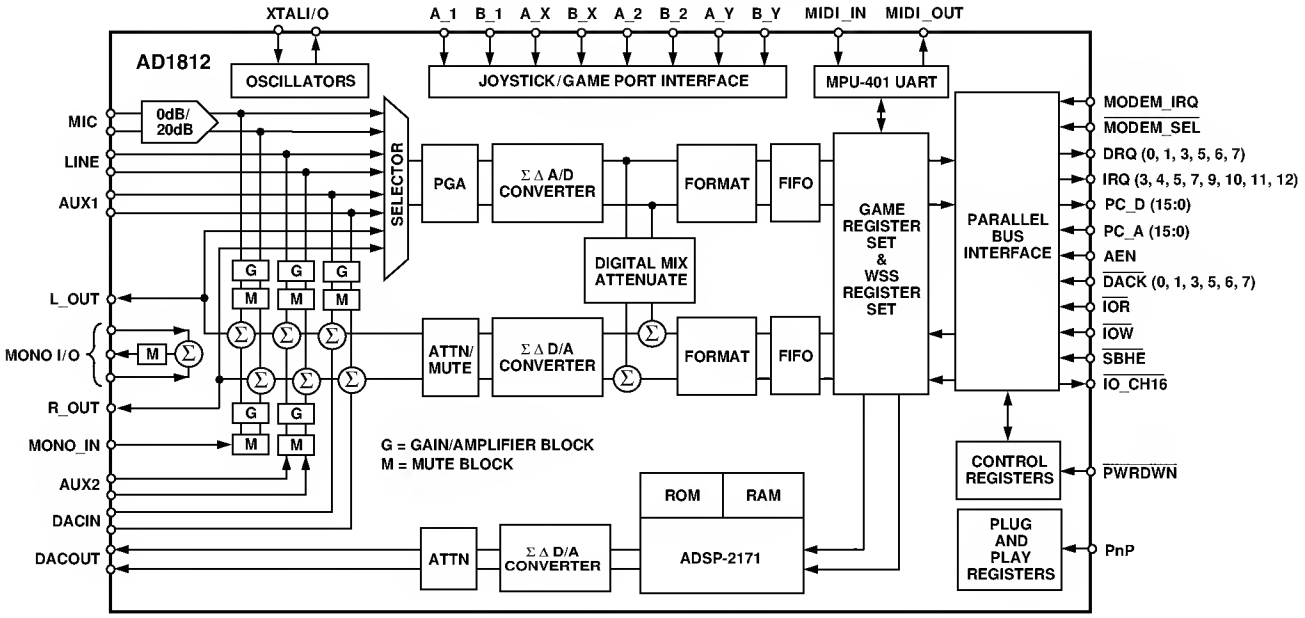
The AD1812 SoundPort® Controller is a single chip audio subsystem for adding 16-bit stereo audio to personal computers. The AD1812 is compatible with Sound Blaster Pro, AdLib, and the Microsoft* Windows Sound System. The AD1812 provides an integrated audio solution for enhanced business audio, entertainment sound effects, and multimedia applications.

The AD1812 audio subsystem combines an integrated digital audio controller, a powerful signal processor, a mixer, and a 16-bit ΣΔ stereo codec. The DOS games register set, the Windows Sound System register set, music synthesis hardware, an MPU-401 compatible UART interface, a game port (with timer), and a Plug and Play ISA interface are all contained on chip. The on-chip Plug and Play (PnP) routine provides configuration services for the internal logical devices and an external modem chipset.

The AD1812 can record compress and playback voice, sound and music. The system provides all PC 95 audio conversion and compatibility requirements for a multimedia enabled PC.

(*continued on Page* 12)

FUNCTIONAL BLOCK DIAGRAM



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AD1812–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

			DAC Test Conditions
Temperature	0	°C	Calibrated
Digital Supply (V_{DD})	5.0	V	0 dB Attenuation
Analog Supply (V_{CC})	5.0	V	Input Full Scale
			16-Bit Linear Mode
Sample Rate (F_S)	48	kHz	10 kΩ Output Load
Input Signal	1008	Hz	Mute Off
Analog Output Passband	20 Hz to 20 kHz		*ADC Test Conditions*
V_{IH}	2.0	V	Calibrated
			0 dB Gain
V_{IL}	0.8	V	Input –1.0 dB Relative to Full Scale
V_{OH}	2.4	V	Line Input Selected
V_{OL}	0.4	V	16-Bit Linear Mode

ANALOG INPUT

Parameter	Min	Typ	Max	Units
Input Voltage (RMS Values Assume Sine Wave Input)				
LINE, AUX1, MONO_IN, AUX2, DACIN		1		V rms
	2.55	2.83	3.11	V p-p
MIC with +20 dB Gain (MGE = 1)		0.1		V rms
	0.250	0.283	0.316	V p-p
MIC with 0 dB Gain (MGE = 0)		1		V rms
	2.55	2.83	3.11	V p-p
Input Impedance*	10	17		kΩ
Input Capacitance*			15	pF

PROGRAMMABLE GAIN AMPLIFIER—ADC

Parameter	Min	Typ	Max	Units
Step Size (0 dB to 22.5 dB) (All Steps Tested)	1.3	1.5	1.7	dB
PGA Gain Range Span	21.5	22.5	23.5	dB

AUXILIARY, LINE, MICROPHONE AND MONO INPUT ANALOG GAIN/AMPLIFIERS/ATTENUATORS

Parameter	Min	Typ	Max	Units
Step Size: AUX1, AUX2, DACIN, LINE, MIC (All Steps Tested)				
(+12 dB to –30 dB)	1.25	1.5	1.75	dB
(–31.5 dB to –34.5 dB)	1	1.5	2.0	dB
Input Gain/Attenuation Range: AUX1, AUX2, DACIN, LINE, MIC	45.0	46.5	47.5	dB
Step Size: MONO_IN (All Steps Tested)				
(0 dB to –39 dB)	2.5	3.0	3.6	dB
(–42 dB to –45 dB)	2.2	3.0	3.85	dB
Input Gain/Attenuation Range: MONO_IN	43	45	46	dB

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

Parameter	Min	Typ	Max	Units
Passband	0		$0.4 \times F_S$	Hz
Passband Ripple			±0.1	dB
Transition Band	$0.4 \times F_S$		$0.6 \times F_S$	Hz
Stopband	$0.6 \times F_S$		∞	Hz
Stopband Rejection	74			dB
Group Delay			$15/F_S$	sec
Group Delay Variation Over Passband			0.0	µs

*Guaranteed not tested.
Specifications subject to change without notice.

ANALOG-TO-DIGITAL CONVERTERS

Parameter	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (–60 dB Input THD+N Referenced to Full Scale, A-Weighted)	80	86		dB
THD+N (Referenced to Full Scale)			0.02	%
		–78	–74	dB
Signal-to-Intermodulation Distortion* (CCIF Method)		80		dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–90	–80	dB
Line to MIC (Input LINE, Ground and Select MIC, Read ADC)		–90	–80	dB
Line to AUX1		–90	–80	dB
Line to AUX2		–90	–80	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error			10	mV

DIGITAL-TO-ANALOG CONVERTERS

Parameter	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (–60 dB Input THD+N Referenced to Full Scale, A-Weighted)	74	81		dB
THD+N (Referenced to Full Scale)			0.022	%
		–77	–73	dB
Signal-to-Intermodulation Distortion* (CCIF Method)			90	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±15	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)		–90	–80	dB
Total Out-of-Band Energy (Measured from $0.6 \times F_S$ to 100 kHz)*			–60	dB
Audible Out-of-Band Energy (Measured from $0.6 \times F_S$ to 20 kHz)*			–70	dB

DAC ATTENUATOR

Parameter	Min	Typ	Max	Units
Step Size (0 dB to –22.5 dB)	1.3	1.5	1.7	dB
Step Size (–22.5 dB to –94.5 dB)*	1.0	1.5	2.0	dB
Output Attenuation Range Span*	93.5	94.5	95.5	dB
Mute Attenuation of 0 dB Fundamental*			80	dB

DIGITAL MIX ATTENUATOR

Parameter	Min	Typ	Max	Units
Step Size (0 dB to –22.5 dB)	1.3	1.5	1.7	dB
Step Size (–22.5 dB to –94.5 dB)*	1.0	1.5	2.0	dB
Digital Mix Attenuation Range Span*	93.5	94.5	95.5	dB

*Guaranteed not tested.
Specifications subject to change without notice.

ANALOG OUTPUT

Parameter	Min	Typ	Max	Units
Full-Scale Output Voltage				
O_L = 0	1.8	2.0	2.2	V p-p
O_L = 1	2.5	2.8	3.11	V p-p
Output Impedance*			600	Ω
External Load Impedance	10			kΩ
Output Capacitance*			15	pF
External Load Capacitance			100	pF
V_{REF}	2.05	2.25	2.45	V
V_{REF} Output Impedance		4		kΩ
Mute Click (Muted Output Minus Unmuted Midscale DAC Output)*			±5	mV

SYSTEM SPECIFICATIONS

Parameter	Min	Typ	Max	Units
System Frequency Response Ripple* (Line In to Line Out)			1.0	dB
Differential Nonlinearity*			±1	LSB
Phase Linearity Deviation*			5	Degrees

STATIC DIGITAL SPECIFICATIONS

Parameter	Min	Typ	Max	Units
High-Level Input Voltage (V_{IH}): Digital Inputs	2			V
Low-Level Input Voltage (V_{IL})			0.8	V
High-Level Output Voltage (V_{OH}), I_{OH} = 24 mA	2.4			V
Low-Level Output Voltage (V_{OL}), I_{OL} = 24 mA			0.4	V
Input Leakage Current	–10		10	µA
Output Leakage Current	–10		10	µA

POWER SUPPLY

Parameter	Min	Typ	Max	Units
Power Supply Range—Analog	4.75		5.25	V
Power Supply Range—Digital	4.75		5.25	V
Power Supply Current			250	mA
Power Dissipation			1.25	W
Analog Supply Current			55	mA
Digital Supply Current			195	mA
Digital Power Supply Current—Power Down			15	mA
Analog Power Supply Current—Power Down			1	mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)*				
(At Both Analog and Digital Supply Pins, Both ADCs and DACs)	40			dB

CLOCK SPECIFICATIONS*

Parameter	Min	Typ	Max	Units
Input Clock Frequency	6	14.31818	18	MHz
Recommended Clock Duty Cycle	10	50	90	%
Power Up Initialization Time			500	ms

*Guaranteed not tested.
Specifications subject to change without notice.

TIMING PARAMETERS (GUARANTEED OVER OPERATING TEMPERATURE RANGE)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{IOW}/\overline{IOR}$ Strobe Width	t_{STW}	100			ns
$\overline{IOW}/\overline{IOR}$ Rising to $\overline{IOW}/\overline{IOR}$ Falling	t_{BWDN}	80			ns
Write Data Setup to $\overline{IOW}$ Rising	t_{WDSU}	10			ns
$\overline{IOR}$ Falling to Valid Read Data	t_{RDDV}			40	ns
AEN Setup to $\overline{IOW}/\overline{IOR}$ Falling	t_{AESU}	10			ns
AEN Hold from $\overline{IOW}/\overline{IOR}$ Rising	t_{AEHD}	0			ns
Adr Setup to $\overline{IOW}/\overline{IOR}$ Falling	t_{ADSU}	10			ns
Adr Hold from $\overline{IOW}/\overline{IOR}$ Rising	t_{ADHD}	10			ns
$\overline{DACK}$ Rising to $\overline{IOW}/\overline{IOR}$ Falling	t_{DKSU1}	20			ns
$\overline{IOW}/\overline{IOR}$ Rising to $\overline{DACK}$ Falling	t_{DKHD1}	0			ns
$\overline{DACK}$ Setup to $\overline{IOW}/\overline{IOR}$ Falling	t_{DKSU2}	10			ns
Data Hold from $\overline{IOR}$ Rising	t_{DHD1}			20	ns
Data Hold from $\overline{IOW}$ Rising	t_{DHD2}	15			ns
DRQ Hold from $\overline{IOW}/\overline{IOR}$ Falling	t_{DRHD}			25	ns
$\overline{DACK}$ Hold from $\overline{IOW}$ Rising	t_{DKHD2}	10			ns
$\overline{DACK}$ Hold from $\overline{IOR}$ Rising	t_{DKHD3}	10			ns

*Guaranteed, not tested.
Specifications subject to change without notice.

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an additional device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times. Note that all 8-bit DMA transfers occur on channels 0, 1, and 3, while all 16-bit DMA transfers occur on channels 5, 6, and 7.

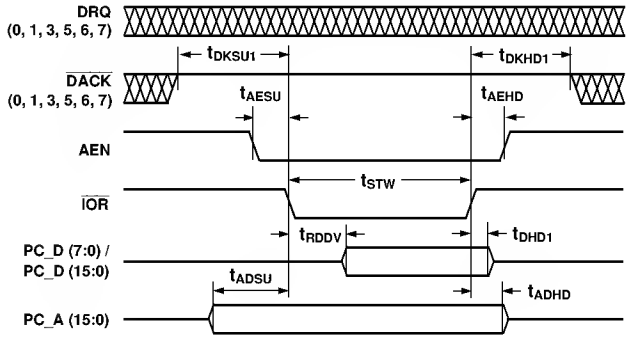


Figure 1. PIO Read Cycle

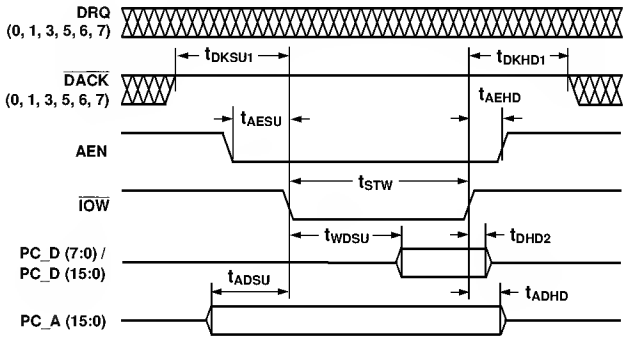


Figure 2. PIO Write Cycle

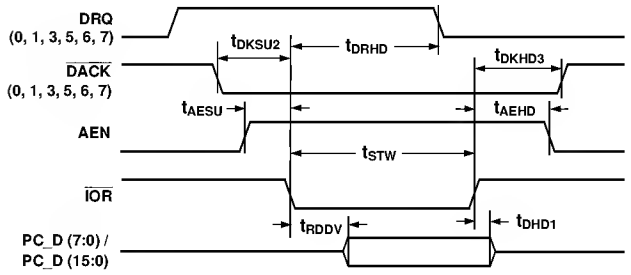


Figure 3. DMA Read Cycle

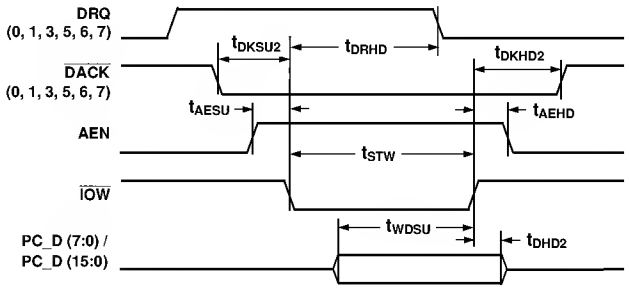


Figure 4. DMA Write Cycle

Table I. Codec Transfer 16-Bit Interface, No Byte Swap (P/CINF8 = 0, P/CBSW = 0)*

Format	Word 1 (16-Bit) MSB		Word 1 (16-Bit) LSB		Word 0 (16-Bit) MSB		Word 0 (16-Bit) LSB	
Mono, 16-Bit Little Endian	Upper 8 Bits of Sample 1 Left Channel		Lower 8 Bits of Sample 1 Left Channel		Upper 8 Bits of Sample 0 Left Channel		Lower 8 Bits of Sample 0 Left Channel	
Stereo, 16-Bit Little Endian	Upper 8 Bits of Sample 0 Right Channel		Lower 8 Bits of Sample 0 Right Channel		Upper 8 Bits of Sample 0 Left Channel		Lower 8 Bits of Sample 0 Left Channel	
Mono, 8-Bit Linear PCM µ-Law PCM A-Law PCM	Sample 3, 8 Bits Left Channel		Sample 2, 8 Bits Left Channel		Sample 1, 8 Bits Left Channel		Sample 0, 8 Bits Left Channel	
Stereo, 8-Bit Linear PCM µ-Law PCM A-Law PCM	Sample 1, 8 Bits Right Channel		Sample 1, 8 Bits Left Channel		Sample 0, 8 Bits Right Channel		Sample 0, 8 Bits Left Channel	
Mono, 4-Bit IMA-ADPCM	Sample 7, 4 Bits Left Channel	Sample 6, 4 Bits Left Channel	Sample 5, 4 Bits Left Channel	Sample 4, 4 Bits Left Channel	Sample 3, 4 Bits Left Channel	Sample 2, 4 Bits Left Channel	Sample 1, 4 Bits Left Channel	Sample 0, 4 Bits Left Channel
Stereo, 4-Bit IMA-ADPCM	Sample 3, 4 Bits Right Channel	Sample 3, 4 Bits Left Channel	Sample 2, 4 Bits Right Channel	Sample 2, 4 Bits Left Channel	Sample 1, 4 Bits Right Channel	Sample 1, 4 Bits Left Channel	Sample 0, 4 Bits Right Channel	Sample 0, 4 Bits Left Channel
Mono, 16-Bit Big Endian	Lower 8 Bits of Sample 1 Left Channel		Upper 8 Bits of Sample 1 Left Channel		Lower 8 Bits of Sample 0 Left Channel		Upper 8 Bits of Sample 0 Left Channel	
Stereo, 16-Bit Big Endian	Lower 8 Bits of Sample 0 Right Channel		Upper 8 Bits of Sample 0 Right Channel		Lower 8 Bits of Sample 0 Left Channel		Upper 8 Bits of Sample 0 Left Channel	

*Regardless of the data format used, the AD1812's codec always transfers 32 bits of data (two 16-bit words).

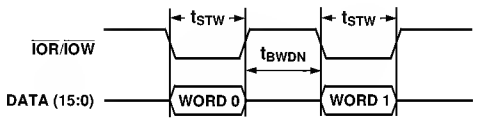


Figure 5. Codec Transfers 16-Bit Interface

Table II. Codec Transfer 16-Bit Interface with Byte Swap (P/CINF8 = 0, P/CBSW = 1)*

Format	Word 1 (16-Bit) MSB		Word 1 (16-Bit) LSB		Word 0 (16-Bit) MSB		Word 0 (16-Bit) LSB	
Mono, 16-Bit Little Endian	Lower 8 Bits of Sample 1 Left Channel		Upper 8 Bits of Sample 1 Left Channel		Lower 8 Bits of Sample 0 Left Channel		Upper 8 Bits of Sample 0 Left Channel	
Stereo, 16-Bit Little Endian	Lower 8 Bits of Sample 0 Right Channel		Upper 8 Bits of Sample 0 Right Channel		Lower 8 Bits of Sample 0 Left Channel		Upper 8 Bits of Sample 0 Left Channel	
Mono, 8-Bit Linear PCM μ-Law PCM A-Law PCM	Sample 2, 8 Bits Left Channel		Sample 3, 8 Bits Left Channel		Sample 0, 8 Bits Left Channel		Sample 1, 8 Bits Left Channel	
Stereo, 8-Bit Linear PCM μ-Law PCM A-Law PCM	Sample 1, 8 Bits Left Channel		Sample 1, 8 Bits Right Channel		Sample 0, 8 Bits Left Channel		Sample 0, 8 Bits Right Channel	
Mono, 4-Bit IMA-ADPCM	Sample 5, 4 Bits Left Channel	Sample 4, 4 Bits Left Channel	Sample 7, 4 Bits Left Channel	Sample 6, 4 Bits Left Channel	Sample 1, 4 Bits Left Channel	Sample 0, 4 Bits Left Channel	Sample 3, 4 Bits Left Channel	Sample 2, 4 Bits Left Channel
Stereo, 4-Bit IMA-ADPCM	Sample 2, 4 Bits Right Channel	Sample 2, 4 Bits Left Channel	Sample 3, 4 Bits Right Channel	Sample 3, 4 Bits Left Channel	Sample 0, 4 Bits Right Channel	Sample 0, 4 Bits Left Channel	Sample 1, 4 Bits Right Channel	Sample 1, 4 Bits Left Channel
Mono, 16-Bit Big Endian	Upper 8 Bits of Sample 1 Left Channel		Lower 8 Bits of Sample 1 Left Channel		Upper 8 Bits of Sample 0 Left Channel		Lower 8 Bits of Sample 0 Left Channel	
Stereo, 16-Bit Big Endian	Upper 8 Bits of Sample 0 Right Channel		Lower 8 Bits of Sample 0 Right Channel		Upper 8 Bits of Sample 0 Left Channel		Lower 8 Bits of Sample 0 Left Channel	

*Regardless of the data format used, the AD1812's codec always transfers 32 bits of data (two 16-bit words).

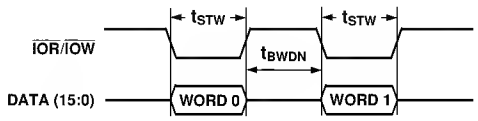


Figure 6. Codec Transfers 16-Bit Interface

Table III. Codec Transfer 8-Bit Interface (P/CINF8 = 1)*

Format	Byte 3 MSB LSB		Byte 2 MSB LSB		Byte 1 MSB LSB		Byte 0 MSB LSB	
Mono, 16-Bit Little Endian	Upper 8 Bits of Sample 1 Left Channel		Lower 8 Bits of Sample 1 Left Channel		Upper 8 Bits of Sample 0 Left Channel		Lower 8 Bits of Sample 0 Left Channel	
Stereo, 16-Bit Little Endian	Upper 8 Bits of Sample 0 Right Channel		Lower 8 Bits of Sample 0 Right Channel		Upper 8 Bits of Sample 0 Left Channel		Lower 8 Bits of Sample 0 Left Channel	
Mono, 8-Bit Linear PCM µ-Law PCM A-Law PCM	Sample 3, 8 Bits Left Channel		Sample 2, 8 Bits Left Channel		Sample 1, 8 Bits Left Channel		Sample 0, 8 Bits Left Channel	
Stereo, 8-Bit Linear PCM µ-Law PCM A-Law PCM	Sample 1, 8 Bits Right Channel		Sample 1, 8 Bits Left Channel		Sample 0, 8 Bits Right Channel		Sample 0, 8 Bits Left Channel	
Mono, 4-Bit IMA-ADPCM	Sample 7, 4 Bits Left Channel	Sample 6, 4 Bits Left Channel	Sample 5, 4 Bits Left Channel	Sample 4, 4 Bits Left Channel	Sample 3, 4 Bits Left Channel	Sample 2, 4 Bits Left Channel	Sample 1, 4 Bits Left Channel	Sample 0, 4 Bits Left Channel
Stereo, 4-Bit IMA-ADPCM	Sample 3, 4 Bits Right Channel	Sample 3, 4 Bits Left Channel	Sample 2, 4 Bits Right Channel	Sample 2, 4 Bits Left Channel	Sample 1, 4 Bits Right Channel	Sample 1, 4 Bits Left Channel	Sample 0, 4 Bits Right Channel	Sample 0, 4 Bits Left Channel
Mono, 16-Bit Big Endian	Lower 8 Bits of Sample 1 Left Channel		Upper 8 Bits of Sample 1 Left Channel		Lower 8 Bits of Sample 0 Left Channel		Upper 8 Bits of Sample 0 Left Channel	
Stereo, 16-Bit Big Endian	Lower 8 Bits of Sample 0 Right Channel		Upper 8 Bits of Sample 0 Right Channel		Lower 8 Bits of Sample 0 Left Channel		Upper 8 Bits of Sample 0 Left Channel	

*Regardless of the data format used, the AD1812's codec always transfers 32 bits of data (two 16-bit words).

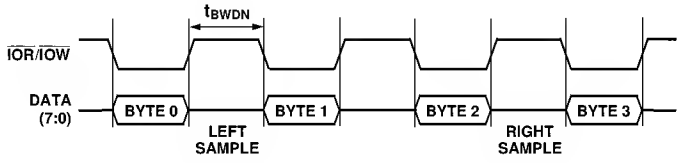


Figure 7. Codec Transfers 8-Bit Interface

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Units
Power Supplies			
Digital (V_{DD})	–0.3	6.0	V
Analog (V_{CC})	–0.3	6.0	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	–0.3	V_{CC} + 0.3	V
Digital Input Voltage (Signal Pins)	–0.3	V_{DD} + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	–65	+150	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

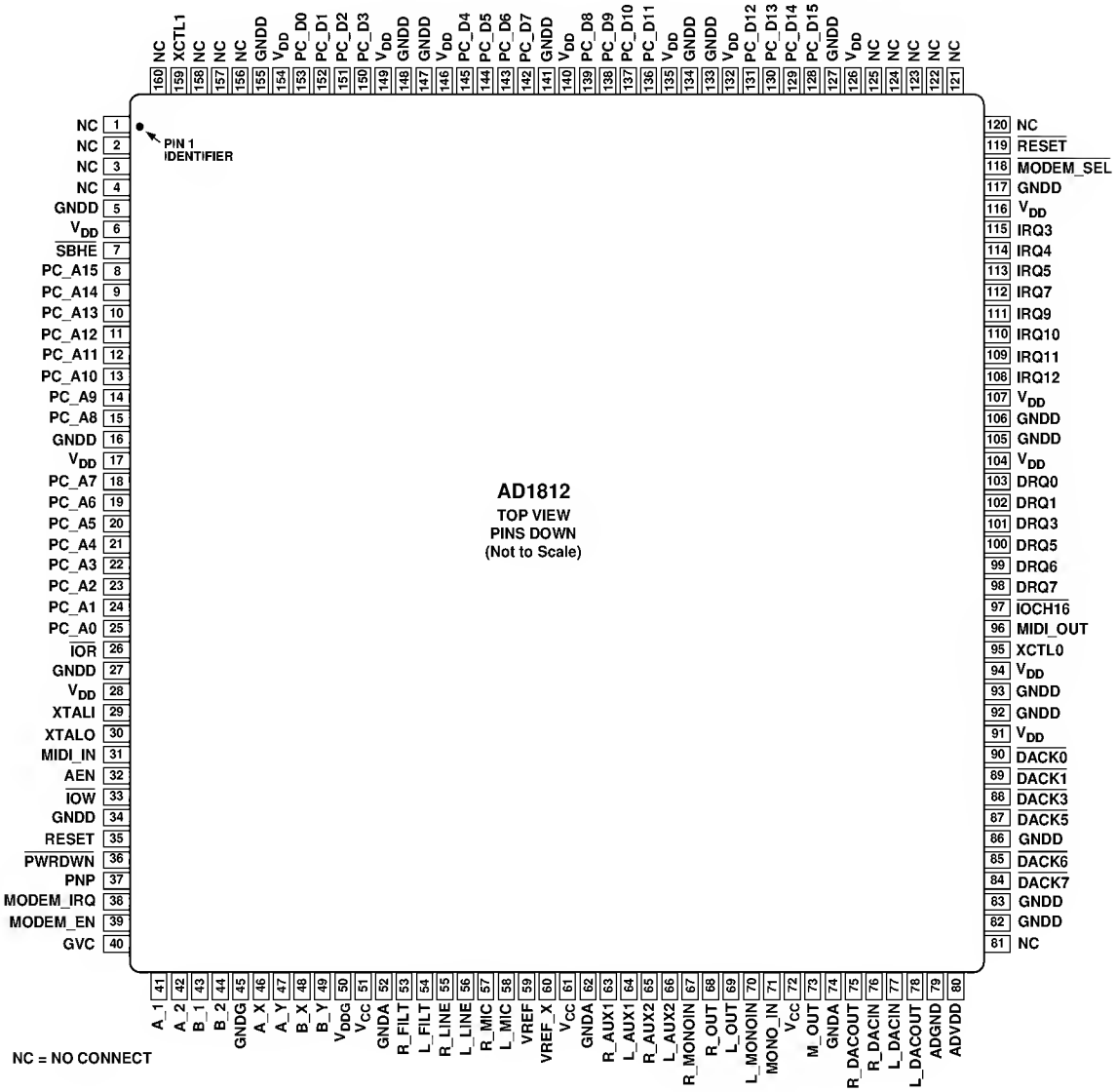
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1812JS	0°C to +70°C	160-Lead PQFP	S-160
AD1812JST	0°C to +70°C	160-Lead TQFP	ST-160

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1812 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PQFP AND TQFP PIN LOCATIONS



PIN DESCRIPTION

Parallel Interface

Pin Name	P/TQFP	I/O	Description
PC_D[15:0]	128–131, 136–139, 142–145, 150–153	I/O	ISA Bus PC Data. PC_D15 to PC_D8 in conjunction with an active HI $\overline{\text{SBHE}}$ connects the AD1812 to the high byte data on the bus, while PC_D7 to PC_D0 connects to the low byte data on the bus.
IRQ(x)	108–115	O	Interrupt Request. IRQ (3, 4, 5, 7, 9, 10, 11, 12). Active HI signals indicating a pending interrupt.
DRQ(x)	98–103	O	DMA Request. DRQ (0, 1, 3, 5, 6, 7). Active HI signals indicating a request for DMA bus operation. DRQ0, DRQ1 and DRQ3 request 8-bit DMA operations while DRQ5, DRQ6 and DRQ7 request 16-bit operations.
PC_A[15:0]	8–15, 18–25	I	ISA Bus PC Address. Connects the AD1812 to the ISA bus address lines.
AEN	32	I	Address Enable. Active HI signal indicates DMA transfer. Active LO signal indicates PIO transfer.
$\overline{\text{DACK}}$ (x)	84–85, 87–90	I	DMA Acknowledge. $\overline{\text{DACK}}$ (0, 1, 3, 5, 6, 7). Active LO signal indicating that a DMA operation can begin.
$\overline{\text{IOR}}$	26	I	I/O Read indicates a read operation.
$\overline{\text{IOW}}$	33	I	I/O Write indicates a write operation.
$\overline{\text{SBHE}}$	7	I	System Byte High Enable. Active LO signal that indicates a byte is being transferred on the upper byte of the 16-bit bus.
$\overline{\text{IOCH16}}$	97	O	IO Channel 16. Active LO signal indicating that one of the logical devices inside the AD1812 is decoded as a 16-bit device.
RESET	35	I	Reset. Active HI.
$\overline{\text{RESET}}$	119	I	Inverted Reset. Active LO.

Analog Signals

Pin Name	P/TQFP	I/O	Description
L_LINE	56	I	Left Line-Level Input.
R_LINE	55	I	Right Line-Level Input.
L_MIC	58	I	Left Microphone Input.
R_MIC	57	I	Right Microphone Input.
L_AUX1	64	I	Left Auxiliary #1 Line-Level Input. Also used for CD input.
R_AUX1	63	I	Right Auxiliary #1 Line-Level Input. Also used for CD input.
L_AUX2	66	I	Left Auxiliary #2 Line-Level Input. Also used for a wavetable input.
R_AUX2	65	I	Right Auxiliary #2 Line-Level Input. Also used for a wavetable input.
L_OUT	69	O	Left Line-Level Output. Left channel post-mixed output.
R_OUT	68	O	Right Line-Level Output. Right channel post-mixed output.
MONO_IN	71	I	Mono Input.
M_OUT	73	O	Mono Output. Sum of L_OUT and R_OUT.
L_DACOUT	78	O	Left DAC Out. Left channel games audio output.
R_DACOUT	75	O	Right DAC Out. Right channel games audio output.
L_DACIN	77	I	Left DAC In. When coupled to L_DACOUT, allows mixing of left channel games audio with left channel audio converted by the codec. The post-mixed output is available on L_OUT.
R_DACIN	76	I	Right DAC In. When coupled to R_DACOUT, allows mixing of right channel games audio with right channel audio converted by the codec. The post-mixed output is available on R_OUT.
L_MONOIN	70	I	Left Mono In. When coupled to L_OUT, M_OUT reflects the left post-mixed output.
R_MONOIN	67	I	Right Mono In. When coupled to R_OUT, M_OUT reflects the right post-mixed output.

Modem Interface Signals

Pin Name	P/TQFP	I/O	Description
MODEM_IRQ	38	I	Modem IRQ. The external modem asserts this pin HI to indicate a pending interrupt. The AD1812 converts this signal to the appropriate interrupt in either Plug and Play (LDN = 5) or Non-Plug and Play mode.
MODEM_EN	39	I	Modem Enable. When this pin is asserted (HI), the AD1812 enables the logical device (LDN = 5) for an external modem chipset. Otherwise, LDN = 5 does not exist. The state of this pin should not be altered after reset.
$\overline{\text{MODEM\_SEL}}$	118	O	Modem Select. This active LO pin is a chip select for an external modem chipset. The AD1812 decodes the (Plug & Play or Non-Plug and Play) configured ISA bus address. AEN must be LO before asserting the MODEM_SEL pin.

Game Port

Pin Name	P/TQFP	I/O	Description
A_1	41	I	Game Port A, Button #1.
A_2	42	I	Game Port A, Button #2.
A_X	46	I	Game Port A X-Axis.
A_Y	47	I	Game Port A Y-Axis.
B_1	43	I	Game Port B, Button #1.
B_2	44	I	Game Port B, Button #2.
B_X	48	I	Game Port B X-Axis.
B_Y	49	I	Game Port B Y-Axis.

MIDI Interface Signals

Pin Name	P/TQFP	I/O	Description
MIDI_IN	31	I	RXD MIDI Input.
MIDI_OUT	96	O	TXD MIDI Output.

Miscellaneous

Pin Name	P/TQFP	I/O	Description
PNP	37	I	Plug and Play Select. When this pin is asserted (HI), the Plug and Play mode is enabled. If PnP is LO, the AD1812 operates in legacy mode, and the Plug and Play configuration is disabled.
XTALO	30	O	14.31818 MHz Crystal Output.
XTALI	29	I	14.31818 MHz Clock Input, can be OSC from the ISA bus.
$\overline{\text{PWRDWN}}$	36	I	Power Down Signal. Active LO.
VREF_X	60	O	Voltage Reference.
VREF	59	I	Voltage Reference Filter.
L_FILT	54	I	Left Channel Filter Input.
R_FILT	53	I	Right Channel Filter Input.
XCTL0	95	O	External Control 0. The state of this pin (TTL HI or LO) is reflected in codec indexed register 0x0A, Bit 6.
XCTL1	159	O	External Control 1. The state of this pin (TTL HI or LO) is reflected in codec indexed register 0x0A, Bit 7.
GVC	40	I	Game Port Voltage Capacitor.
NC	1–4, 81, 120–125, 156–158, 160		No Connect.

Power Supplies

Pin Name	P/TQFP	I/O	Description
V_{CC}	51, 61, 72	I	Analog Supply Voltage (+5 V).
GNDA	52, 62, 74	I	Analog Ground.
V_{DD}	6, 17, 28, 91, 94, 104, 107, 116, 126, 132, 135, 140, 146, 149, 154	I	Digital Supply Voltage (+5 V).
GNDD	5, 16, 27, 34, 82, 83, 86, 92, 93, 105, 106, 117, 127, 133, 134, 141, 147, 148, 155	I	Digital Ground.
ADVDD	80	I	Analog/Digital Supply Voltage. Connect to +5 V_{CC}.
ADGND	79	I	Analog/Digital Ground. Connect to analog ground plane.
V_{DDG}	50	I	Game Port Digital Voltage Supply. Connect to +5 V_{DD}.
GNDG	45	I	Game Port Digital Ground. Connect to the digital ground plane.

(continued from Page 1)

HOST PC INTERFACE

All necessary ISA bus interface logic is completely contained on-chip. This includes address decoding for all onboard resources, control and signal interpretation, DMA selection and control logic, IRQ selection and control logic, and all interface configuration logic (see Table IV).

The AD1812 supports a DMA request/grant architecture for transferring data with the ISA bus. One, two, or three DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. The AD1812 includes dual DMA count registers for full-duplex operation enabling simultaneous capture and playback on separate DMA channels.

The AD1812 is fully configurable according to the Plug and Play ISA specification. In a non-Plug and Play environment, the built in Plug and Play protocol can be disabled. When Plug and Play is disabled, the AD1812 operates under a fixed address space.

Table IV. Emulated Logical Devices

Logical Device Number	Emulated Device	PnP Compatible Device
0	Windows Sound System	—
1	Sound Blaster Pro v. 2.01	PNPB002
2	OPL3 Music Synthesizer	PNPB020
3	MIDI MPU-401 Port	PNPB006
4	Game/Joystick Port	PNPB02F
5*	Modem	PNP0501

*If MODEM_EN is asserted.

WSS COMPATIBLE CODEC

The AD1812 contains the AD1845 SoundPort Stereo Codec for business audio support and multimedia applications. The codec includes stereo audio converters, complete on-chip filtering, MPC Level-2 compliant analog mixing, programmable gain and attenuation, a variable sample frequency generator, and FIFOs buffering the ISA bus.

The codec includes a stereo pair of ∑Δ analog-to-digital converters and a stereo pair of ∑Δ digital-to-analog converters. Inputs to the ADC can be selected from four stereo pairs of analog signals: line (LINE), microphone (MIC), auxiliary line #1 (AUX1), and post-mixed DAC output. In addition, an analog mixer allows a mono input (MONO_IN), MIC, AUX1, LINE and auxiliary line #2 (AUX2) to be mixed with the DACs' output. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

The pair of 16-bit outputs from the ADCs are available over a 16-bit bidirectional interface that also supports 16-bit digital input to the DACs and control information. The codec can accept and generate 16-bit twos-complement PCM linear (big endian or little endian) digital data, 4-bit IMA-ADPCM compatible digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

The AD1812 includes a variable sample frequency generator, which allows the codec to instantaneously change sample rates from 5.5 kHz to 50 kHz with a resolution of 1 Hz. This is a superb way to create special audio effects.

SOUND BLASTER EMULATION

Sound Blaster emulation is provided using a combination of the embedded signal processor and dedicated hardware. All Sound Blaster Pro version 2.01 functions are supported including record. The hardware registers are fully implemented within the AD1812, and the internal signal processor executes a command controller to interpret all commands. The AD1812 uses the internal signal processor for decoding compressed files compatible with Sound Blaster ADPCM.

MUSIC SYNTHESIZER EMULATION

The AD1812 includes an embedded signal processor based on Analog Devices' 16-bit fixed-point digital signal processor family. All DSP instructions are ROM coded internally. The

music synthesis algorithm running on the signal processor emulates the functions of industry standard OPL3 FM synthesizer chips and delivers 20 voice polyphony. A dedicated pair of ∑Δ DACs converts the digitally synthesized music before mixing with the AD1812 codec line output.

EuSynth-1+ was developed by EuPhonics, a research and product development company that specializes in audio processing and electronic music synthesis.

MPU-401 INTERFACE

The primary interface for communicating MIDI data to and from the host PC is the emulated MPU-401 interface. The MPU-401 interface includes has a built-in FIFO for communicating to the host bus.

GAME PORT INTERFACE

An IBM-compatible game port interface is provided on-chip. The game port is capable of supporting up to two joysticks. Connecting the game port to a 15-pin D-sub connector requires only a few capacitors and resistors. The AD1812 includes a built-in game port timer.

MODEM INTERFACE

Asserting the MODEM_EN pin on the AD1812 provides chip select, interrupt handling and address decoding for an external modem chipset. The AD1812 decodes the modem ISA bus address and issues a modem select on the MODEM_SEL pin. Interrupts generated by the external modem are handled on the MODEM_IRQ pin, converted to the assigned system interrupt by the AD1812, and posted to the ISA bus. The modem interface operates in a PnP or non-PnP enabled system.

PLUG AND PLAY (PnP)

The AD1812 can be used under PnP control or in a non-PnP mode. The non-PnP registers mimic the PnP register set, except for the user defined addresses for the PnP "ADDRESS" and "WRITE_DATA" registers. The PnP registers are selected by asserting the PnP pin. With the PnP pin deasserted, the non-PnP registers are selected.

Table V. Plug and Play Registers (PNP Asserted)

Port Name	Location	Type
ADDRESS	0x279 (Printer Status Port)	Write-Only
WRITE_DATA	0xA79 (Printer Status Port + 0x800)	Write-Only
READ_DATA	Relocatable in Range 0x203 – 0x3FF	Read-Only

Table VI. Non-Plug and Play Registers (PNP Deasserted)

Port Name	Location	Type
ADDRESS	0x234	Write-Only
WRITE_DATA	0x235	Write-Only
READ_DATA	Relocatable in Range 0x203 – 0x3FF	Read-Only

PnP AD1812 (Card) Status

For cards in PnP mode (PnP_Enable asserted), the Plug and Play ISA Specification describes how to transfer the AD1812 from its start-up state, "Wait For Key" State, to the configuration state, "Config" State. In the configuration state, the I/O ranges, interrupt channels, and DMA channels can be assigned.

For non-PnP operation, no initialization protocol is needed because the card is locked in the configuration state.

Configuration Register Description

The following describes only the subset of PnP Registers that are unique to the AD1812 or necessary for non-PnP operation. All other PnP registers are described in the Plug and Play ISA Specification.

A register is selected by performing an 8-bit I/O write to the ADDRESS Port, followed by either a read from the READ_DATA location or a write to the WRITE_DATA location. Successive reads or writes to a single register can be done without rewriting the ADDRESS register. The following are valid values for the ADDRESS Port.

Table VII. PnP Address Port Registers

Register Name	Address Value	Type	Description
RD_DATA Port	0x00	Write-Only	Sets the value of the READ_DATA Port.
Config Control	0x02	Write-Only	Resets all logical devices.
Logical Device Number	0x07	Read/Write	Selects current logical device.
Powerdown	0x20	Read/Write	Manages power for portions of the AD1812.

Table VIII. Windows Sound System, Logical Device Number = 0

Register Name	Address	Type	Description Value
Activate	0x30	Read/Write	Activates device.
I/O Range Check	0x31	Read/Write	Performs conflict check on selected I/O range.
I/O Port Base	0x60	Read/Write	I/O Base [15:8].
Address	0x61	Read/Write	I/O Base [7:0].
IRQ Level Select	0x70	Read/Write	Selects interrupt level.
IRQ Type Select	0x71	Read-Only	Active HI, level-sensitive (not user programmable).
DMA Select 0	0x74	Read/Write	Indicates DMA capture channel.
DMA Select 1	0x75	Read/Write	Indicates DMA playback channel. (If DMA 0 is not used, capture and playback occurs on DMA 1.)

Table IX. Game Registers, Logical Device Number = 1

Register Name	Address Value	Type	Description
Activate	0x30	Read/Write	Activates device.
I/O Range Check	0x31	Read/Write	Performs conflict check on selected I/O range.
I/O Port Base	0x60	Read/Write	I/O Base [9:8].
Address	0x61	Read/Write	I/O Base [7:0].
IRQ Level Select	0x70	Read/Write	Selects interrupt level.
IRQ Type Select	0x71	Read-Only	Active HI, edge-sensitive (not user programmable).
DMA Select 0	0x74	Read/Write	Indicates which 8-bit DMA channel.

Table X. Music Synthesizer, Logical Device Number = 2

Register Name	Address Value	Type	Description
Activate	0x30	Read/Write	Activates device.
I/O Range Check	0x31	Read/Write	Performs conflict check on selected I/O range.
I/O Port Base	0x60	Read/Write	I/O Base [9:8].
Address	0x61	Read/Write	I/O Base [7:0].

Table XI. MIDI Port, Logical Device Number = 3

Register Name	Address Value	Type	Description
Activate	0x30	Read/Write	Activates device.
I/O Range Check	0x31	Read/Write	Performs conflict check on selected I/O range.
I/O Port Base	0x60	Read/Write	I/O Base [9:8].
Address	0x61	Read/Write	I/O Base [7:0].
IRQ Level Select	0x70	Read/Write	Selects interrupt level.
IRQ Type Select	0x71	Read-Only	Active HI, edge-sensitive (not user programmable).

Table XII. Game Port, Logical Device Number = 4

Register Name	Address Value	Type	Description
Activate	0x30	Read/Write	Activates device.
I/O Range Check	0x31	Read/Write	Performs conflict check on selected I/O range.
I/O Port Base	0x60	Read/Write	I/O Base [9:8].
Address	0x61	Read/Write	I/O Base [7:0].

Table XIII. Modem, Logical Device Number = 5

Register Name	Address Value	Type	Description
Activate	0x30	Read/Write	Activates device.
I/O Range Check	0x31	Read/Write	Performs conflict check on selected I/O range.
I/O Port Base	0x60	Read/Write	I/O Base [9:8].
Address	0x61	Read/Write	I/O Base [7:0].
IRQ Level Select	0x70	Read/Write	Selects interrupt level.
IRQ Type Select	0x71	Read Only	Active HI, edge-sensitive (not user programmable).

Power-Down Control

The AD1812 contains two levels of Power-Down control. One level of control is accessed through the embedded codec registers and another is accessed via the PnP vendor defined registers.

The codec registers allow sections of the embedded codec to be turned off to conserve power.

Table XIV. Codec Power-Down Modes

Mode	Powered-Down Blocks
Total Power Down	ADC, DAC, Mixer, Reference
Standby	ADC, DAC, Mixer
Mixer Power Down	DAC, Mixer
Mixer Only	ADC, DAC
ADC Power Down	ADC
DAC Power Down	DAC

The registers found in the vendor defined PnP space take precedence over any other power-down mode. You can shut down the embedded DSP or the entire codec by writing to these registers.

Table XV. PnP Power-Down Modes

Mode	Powered-Down Blocks
Total Power Down	DSP and SoundPort Codec

CODEC CONTROL REGISTER ARCHITECTURE

Upon Plug and Play initialization, a base address is assigned for the Windows Sound System Compatible logical device embedded in the AD1812. The AD1812 accepts both data and control information through the 16-bit interface.

Table XVI. Codec Direct Register Map

Windows Sound System Address	Register Name
Base + 0	Index Address Register
Base + 2	Indexed Data Register
Base + 4	Status Register
Base + 6	PIO Data Registers

A write to or a read from the Indexed Data Register will access the Indirect Register which is selected by the value most recently written to the Index Address Register. The Status Register and the PIO Data Register are always accessible directly, without indexing. The 32 Indirect Registers are shown in Table XVII.

Table XVII. Codec Indirect Register Map

Windows Sound System Codec Indexed Register	Index	Reset State
Left Input Control	0x00	0x80
Right Input Control	0x01	0x80
Left Aux #1 Input Control	0x02	
Right Aux #1 Input Control	0x03	0x9F
Left Aux #2 Input Control	0x04	0x9F
Right Aux #2 Input Control	0x05	0x9F
Left Output Control	0x06	0xBF
Right Output Control	0x07	0xBF
Clock and Data Format	0x08	0x08
Interface Configuration	0x09	0x00
Pin Control	0x0A	0x05
Test and Initialization	0x0B	0x20
Miscellaneous Information	0x0C	0xCA
Digital Mix/Attenuation	0x0D	0x00
Upper Base Count	0x0E	0x00
Lower Base Count	0x0F	0x00
Alternate Feature Enable/Left MIC Input Control	0x10	0x80
MIC Mix Enable/Right MIC Input Control	0x11	0x00
Left Line Gain, Attenuate, Mute, Mix	0x12	0x9F
Right Line Gain, Attenuate, Mute, Mix	0x13	0x9F
Lower Timer	0x14	0x00
Upper Timer	0x15	0x00
Upper Frequency Select	0x16	0x2A
Lower Frequency Select	0x17	0xF8
External Status	0x18	0x30
Revision ID	0x19	0x80
Mono Control	0x1A	0xC0
Power-Down Control	0x1B	0x08
Capture Data Format Control	0x1C	0x50
Total Power-Down	0x1D	0x00
Capture Upper Base Count	0x1E	0x00
Capture Lower Base Count	0x1F	0x00

A detailed map of all direct and indirect register contents is summarized for reference as follows:

Table XVIII. Codec Direct Registers (16-Bit Interface)

Direct Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WSS Base	res	res	res	res	res	res	res	res	INIT	MCE	TRD	IXA4	IXA3	IXA2	IXA1	IXA0
WSS Base+2	res	res	res	res	res	res	res	res	IXD7	IXD6	IXD5	IXD4	IXD3	IXD2	IXD1	IXD0
WSS Base+4	res	res	res	res	res	res	res	res	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT
WSS Base+6 (read)	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
WSS Base+6 (write)	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Table XIX. Codec Indirect Registers

Indirect Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0
0x01	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0
0x02	LMX1	res	res	LX1A4	LX1A3	LX1A2	LX1A1	LX1A0
0x03	RMX1	res	res	RX1A4	RX1A3	RX1A2	RX1A1	RX1A0
0x04	LMX2	res	res	LX2A4	LX2A3	LX2A2	LX2A1	LX2A0
0x05	RMX2	res	res	RX2A4	RX2A3	RX2A2	RX2A1	RX2A0
0x06	LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
0x07	RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
0x08	PFMT1	PFMT0	PC/L	PS/M	PBSW	PINF8	res	res
0x09	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN
0x0A	XCTL1	XCTL0	res	res	res	res	IEN	res
0x0B	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
0x0C	MID	res	res	res	ID3	ID2	ID1	ID0
0x0D	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME
0x0E	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
0x0F	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0
0x10	OL	TE	LMG4	LMG3	LMG2	LMG1	LMG0	DACZ
0x11	LMME	RMME	RMG4	RMG3	RMG2	RMG1	RMG0	res
0x12	LLM	res	res	LLG4	LLG3	LLG2	LLG1	LLG0
0x13	RLM	res	res	RLG4	RLG3	RLG2	RLLG1	RLG0
0x14	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
0x15	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
0x16	FU7	FU6	FU5	FU4	FU3	FU2	FU1	FU0
0x17	FL7	FL6	FL5	FL4	FL3	FL2	FL1	FL0
0x18	res	TI	CI	PI	CU	CO	PO	PU
0x19	V2	V1	V0	res	res	CID2	CID1	CID0
0x1A	MIM	MOM	res	res	MIA3	MIA2	MIA1	MIA0
0x1B	ADCPWD	DACPWD	MIXPWD	res	res	res	res	res
0x1C	CFMT1	CFMT0	CC/L	CS/M	CBSW	CINF8	res	res
0x1D	res	res	res	res	res	res	res	TOTPWD
0x1E	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
0x1F	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

Note that the only sticky bit in any of the Codec control registers is the interrupt (INT) bit. All other bits change with every sample period.

SYSTEM TIMING AND CONTROL

If the AD1812 is not connected directly to the OSC clock on the ISA bus, a single fundamental-mode and parallel-tuned 14.31818 MHz crystal oscillator can be substituted to derive all timing parameters. Future feature enhanced, pin-compatible versions of the SoundPort Controller will require a 33 MHz clock or crystal input. Analog Devices suggests developing board layouts that can be easily modified to supply the new clock.

DATA AND CONTROL TRANSFERS

The embedded SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with the host computer bus. One or two 8-bit or 16-bit DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. PIO transfers can be made on one channel while the other is performing DMA. Transfers to and from the AD1812 are asynchronous relative to the internal data conversion clock. Transfers are buffered by FIFOs located in the capture and playback paths.

REFERENCE DESIGNS AND DEVICE DRIVERS

Reference designs and device drivers using the AD1812 are available via Bulletin Board Service. The Computer Products Division runs a BBS that can be reached at speeds up to 14,400 baud, no parity, 8 bits data, 1 stop bit, by dialing (617) 461-4258. The BBS supports: V.32bis, error correction (V.42 and MNP classes 2, 3, and 4), and data compression (V.42bis and MNP class 5). Reference designs can also be found in the AD1812 SoundPort Controller Technical Reference which can be obtained by contacting your local Analog Devices sales representative or authorized distributor. You can also find us on the World Wide Web at http://www.analog.com.

FREQUENCY RESPONSE PLOTS

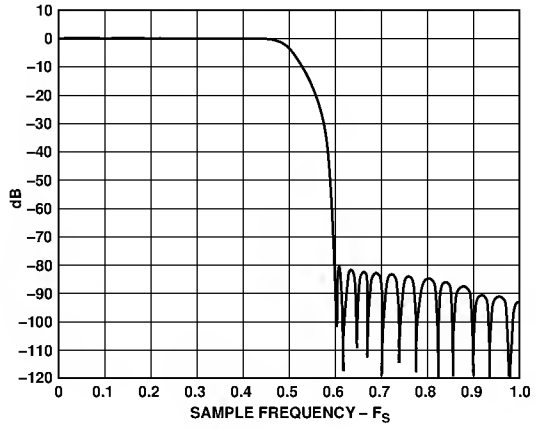


Figure 8. Analog-to-Digital Frequency Response to F_S (Full-Scale Line-Level Inputs, –1 dB Gain)

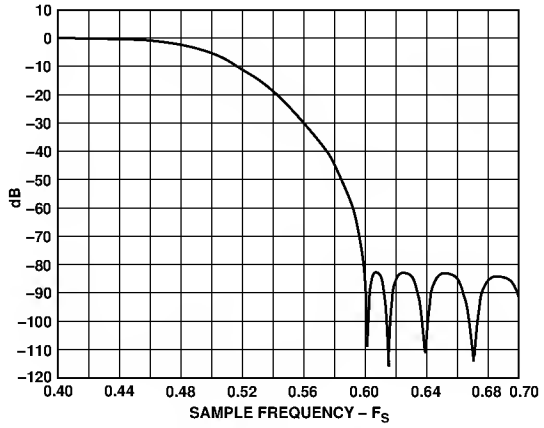


Figure 9. Analog-to-Digital Frequency Response — Transition Band (Full-Scale Line-Level Inputs, –1 dB Gain)

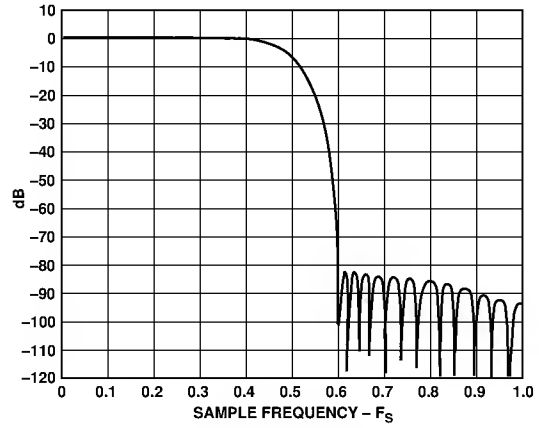


Figure 10. Digital-to-Analog Frequency Response to F_S (Full-Scale Inputs, 0 dB Attenuation)

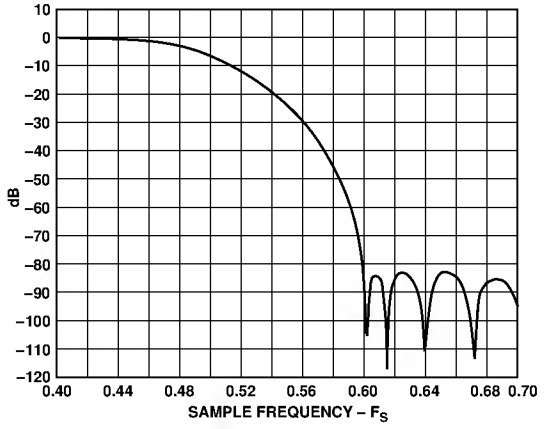


Figure 11. Digital-to-Analog Frequency Response — Transition Band (Full-Scale Inputs, 0 dB Attenuation)

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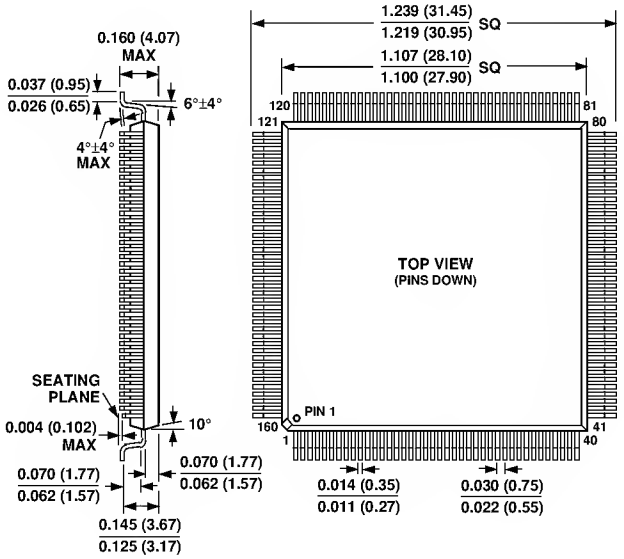
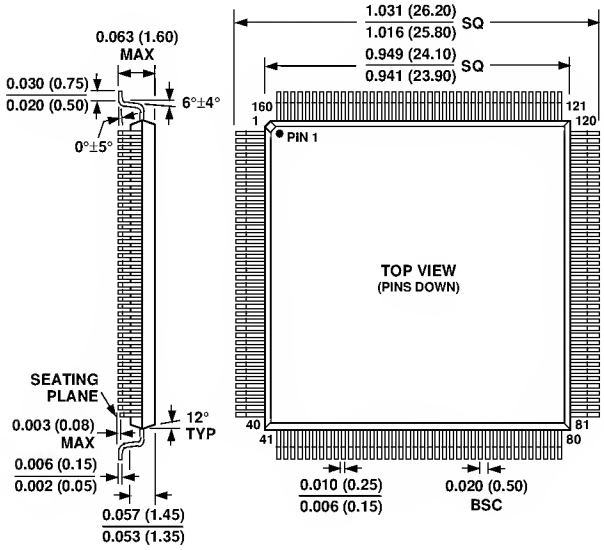
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

160-Lead PQFP
(S-160)



160-Lead TQFP
(ST-160)



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